The questions on this worksheet have been taken from the OCR A-Level Computer Science Practice Paper 1.1

"3-a-day" A-Level Exam Practice Unit 1 (020)

Question 1

The following is a program written using the Little Man Computer instruction set.

```
start  LDA   one
       OUT
       LDA   zero
       OUT
       LDA   count
       SUB   one
       STA   count
       BRP   start
       HLT
one    DAT   1
zero   DAT   0
count  DAT   3
```

Explain the buses and registers used when the line `SUB one` is executed.

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.....[5]

Question 2

Explain, giving an example, how pipelining in a CPU could speed up the execution of this program.

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.....[3]

Question3

Describe **one** issue the line `BRP start` may cause for a CPU using pipelining.

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.....[2]

Pipelining is one factor that affects the performance of a CPU. Identify **one** other factor.

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.....[1]

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Answer 1

- The address of `one` is stored in the MAR - This value is sent along the address bus AND the fetch signal is sent on the control bus. - The contents of `one` are sent from memory to the processer on the data bus and stored in the MDR - The contents of the MDR and ACC are sent to the ALU - The result is stored back in the ACC (1 per -)	**AO2.2** **5**	Accept MBR instead of MDR

Answer 2

- An instruction can be fetched as the previous one is being decoded… - …and the one before that is being executed. - E.g. `LDA Zero` can be fetched, while `OUT` is being	**AO1.2** **(2)**
decoded and `start LDA one` is being executed. (1 per -)	**AO2.2** **(1)**

Answer 3

- BRP could be followed by one of two possible instructions, which one will only be determined at execution - Meaning the wrong one may be fetched/decoded (1 per -)	**AO2.2** **2**
- Clock speed - Cache Size - Number of cores (1 per max 1)	**AO1.1** **1**