The answers on this worksheet have been taken from the 2018 OCR GCSE Computer Science Paper 1

6-A-Day – Computer Science GCSE (p1.8-2016)

Q1	1 mark per bullet to max 2 per register • MAR // memory address register • Stores the address/location where data will be **read/written/accessed/fetched** // address/location of data/instruction being **processed** // address/location of data/instruction next to be **processed** • MDR // memory data register • Stores the data/instruction that is **fetched/read** from memory // stores the data that is to be written to memory // stores the data/instruction from the address in the MAR // data/instruction next to be **processed** • Program counter • Stores the address/location of the next instruction to be run // stores the address/location of the current instruction being run • Accumulator • Stores the result of manipulation/process/calculation	4 AO1 1a (2) AO1 1b (2)	MAR stores address is not enough for description MDR stores the data is not enough for description Allow: • Current instruction register // IR • Stores the instruction currently being processed Accept MBR // Memory buffer register for MDR
Q2	1 mark per bullet to max 2 • The number of FDE cycles run per given time/second // the frequency that the clock 'ticks' • 3.8 billion cycles/instructions … • …per second	2 AO1 1b (1) AO2 1a (1)	Do not award: how fast the computer is // speed of CPU 3.8 = 3,800,000,000
Q3	1 mark per bullet to max 3 e.g. • Software may be designed to run on 1 core and not multiple cores // depends on the task(s) • …some tasks cannot be split across cores • Clock speed also affects speed // dual core may have a faster clock speed // quad-core may have slower clock speed • ….so one task may be run faster/slower • RAM size also affects speed // Quad-core may have less RAM // amount of VM being used • Cache size also affects speed // Quad-core may have less cache	3 AO1 1b (1) AO2 2b (2)	Allow marks for other components that could affect the speed e.g. secondary storage access speed, onboard GPU. Award description of concurrent processing.
Q4	1 mark per bullet to max 3 • VM is used when RAM is full • ...part of the secondary storage used as (temporary) RAM/VM • Data from RAM is moved to the secondary storage/VM (to make space in RAM) • RAM can then be filled with new data • When data in VM is needed it is moved back to RAM	3 AO2 1a (1) AO2 1b (2)	Many candidates are giving disadvantages of VM, or that the computer can now run more programs, which are NAQ
Q5	1 mark per bullet to max 2 • More RAM will improve the performance of the computer // More RAM will speed up the access to data • Excessive use can cause disk thrashing … • …which decreases performance • VM is slower to access than RAM direct (because it has to go back to RAM first) • Moving data between RAM and VM takes processor time	2 AO2 1b (2)	Do not award: VM is slower, without quantifying slower at what
Q6	• An agreement / set of rules / standard • …for how computers should communicate // how data is sent/received/transmitted on a network • Example of what could be agreed in the protocol (e.g. speed / error checking / etc.)	2 AO2 1b (2)	Do not award set of instructions for bullet 1